

FIG.1(a)

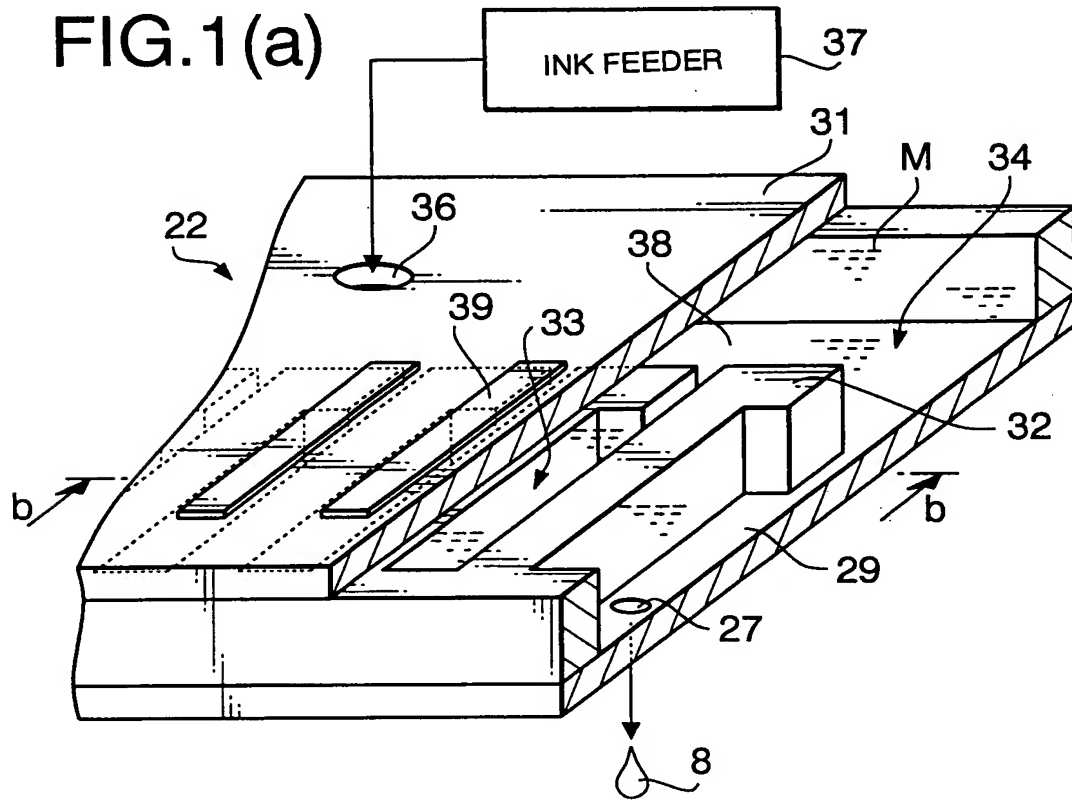


FIG.1(b)

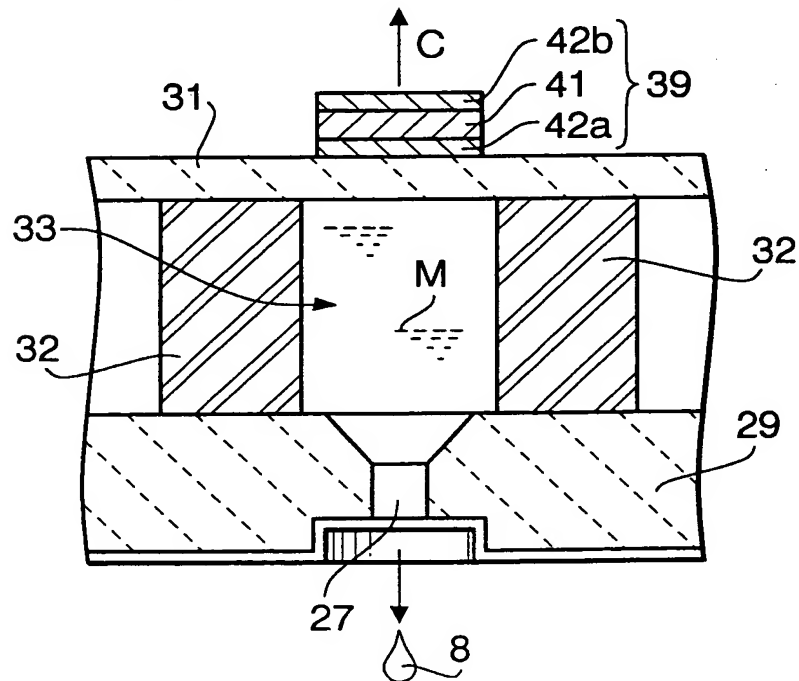


FIG.2(a)

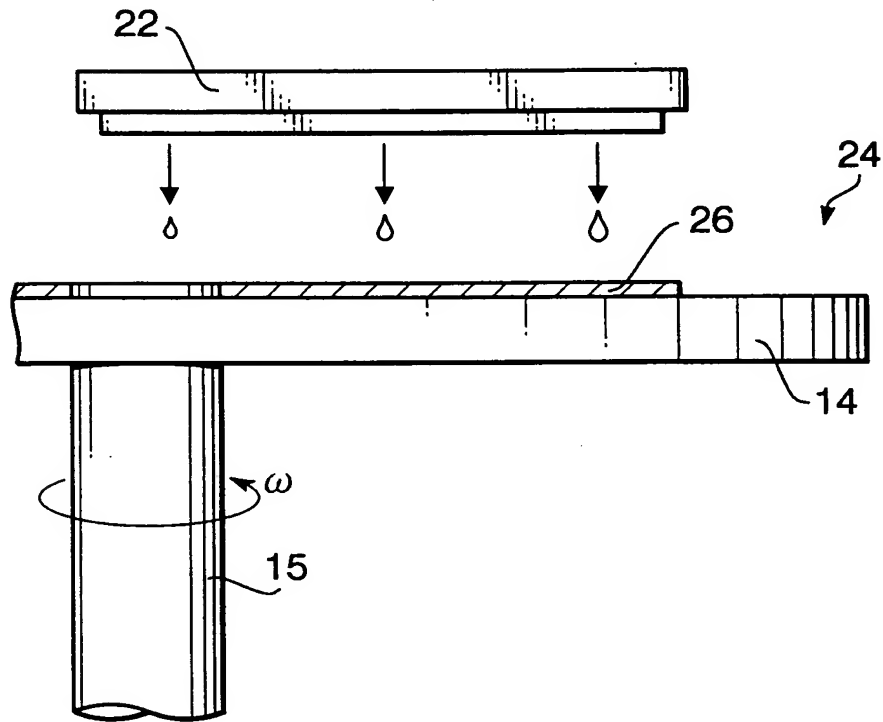


FIG.2(b)

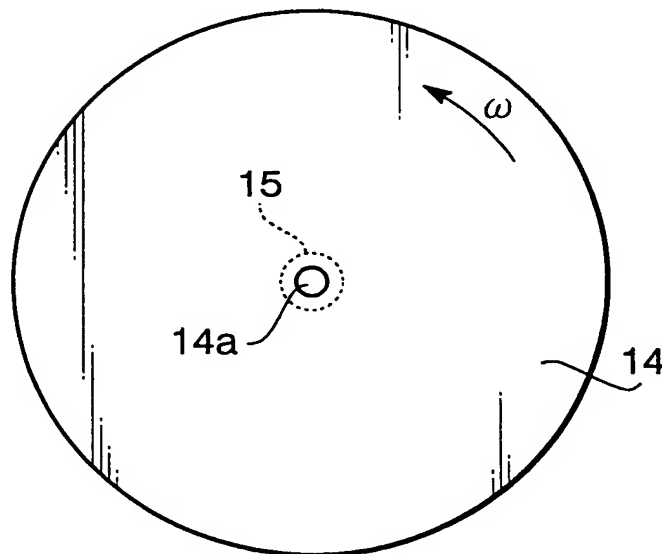


FIG. 3

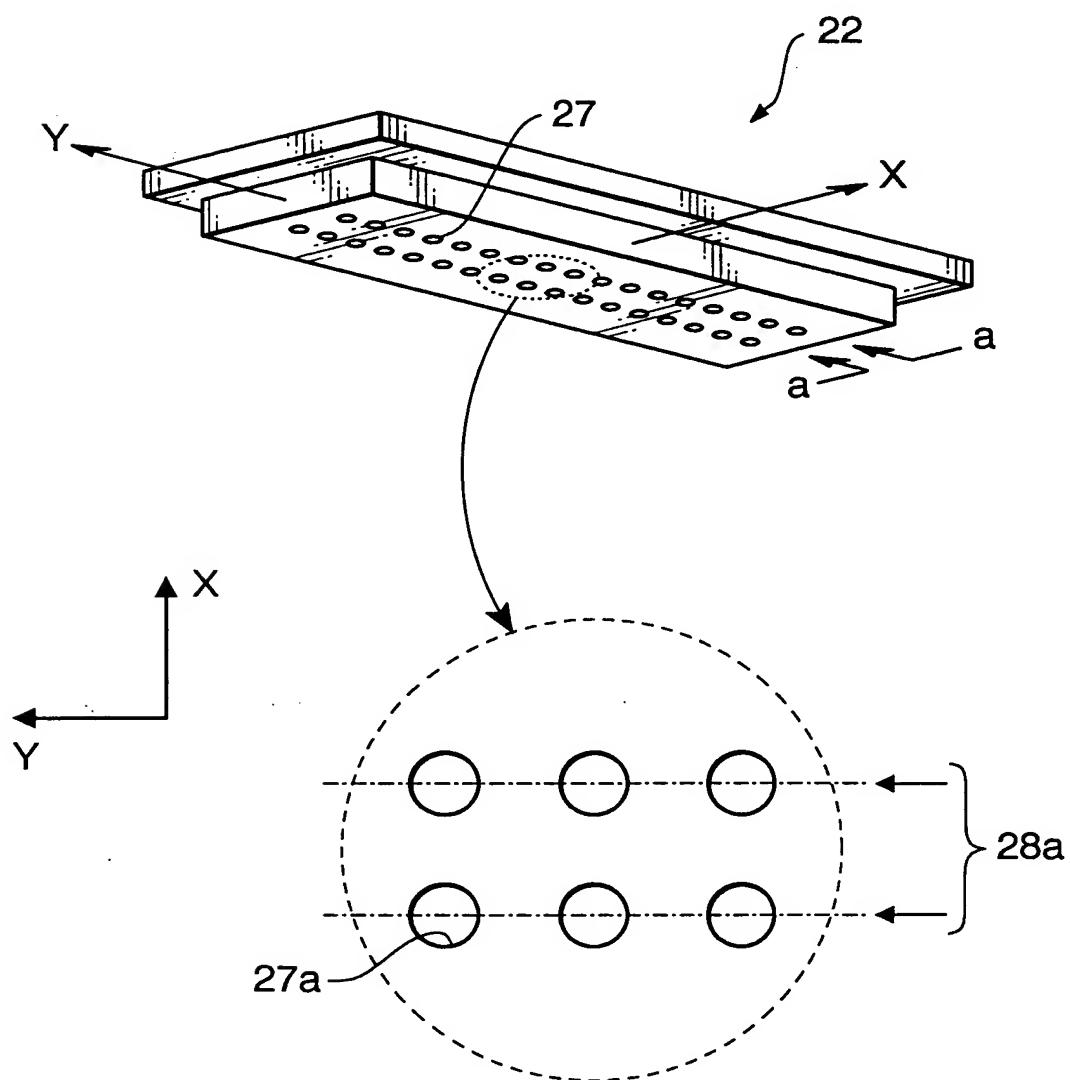


FIG. 4

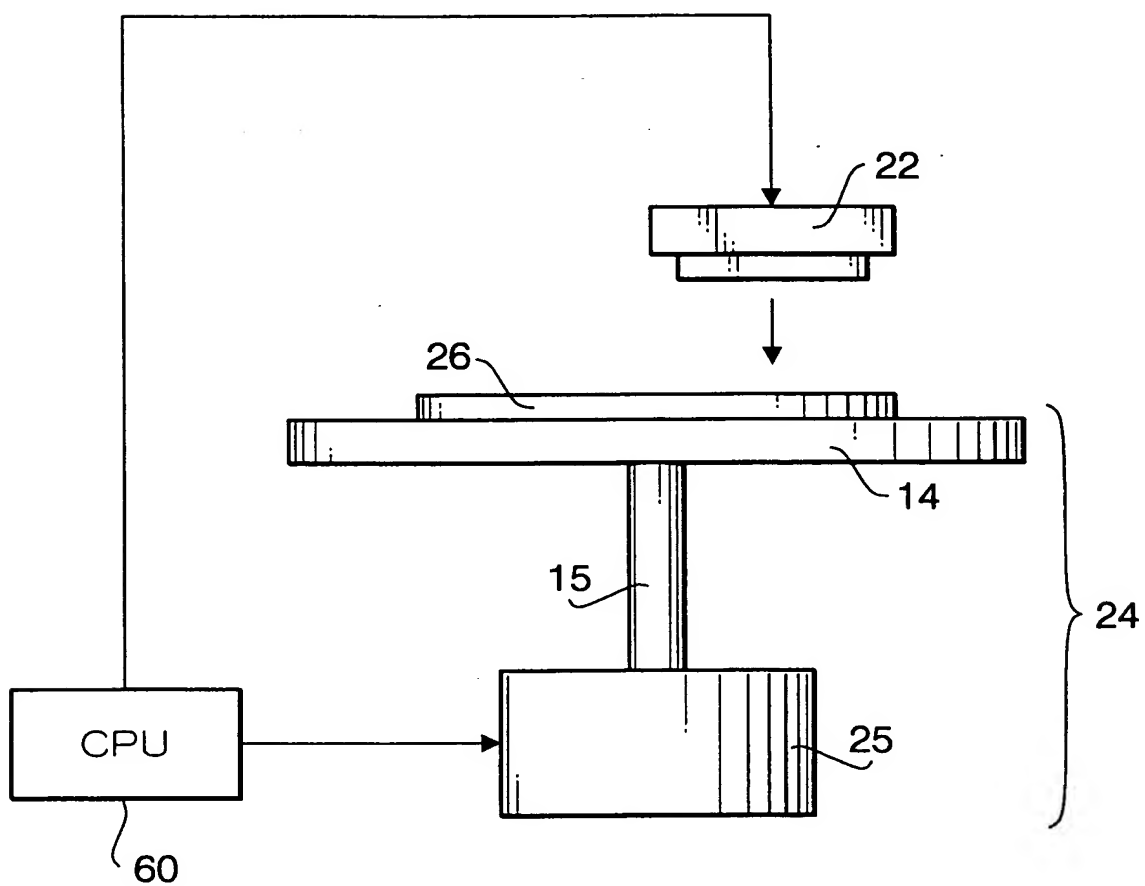


FIG.5(a)

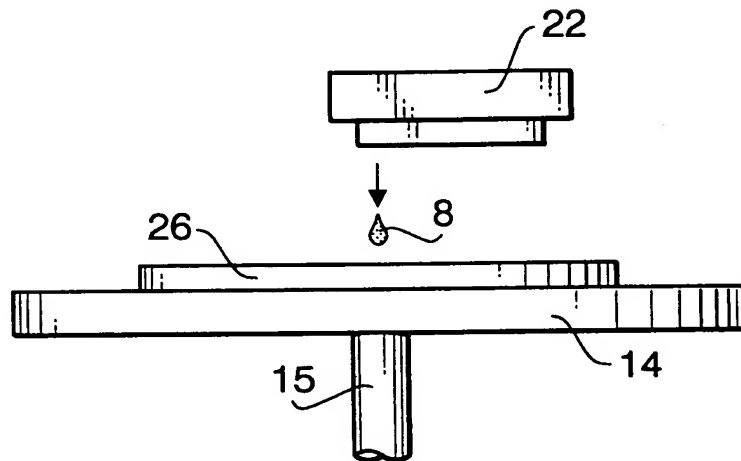


FIG.5(b)

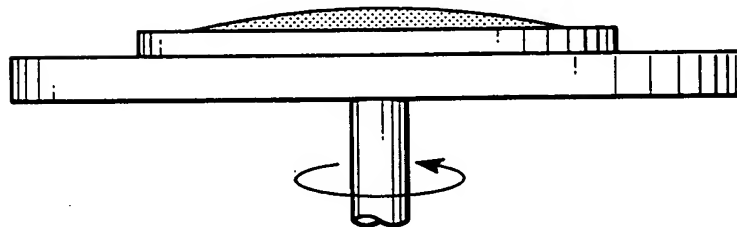


FIG.5(c)

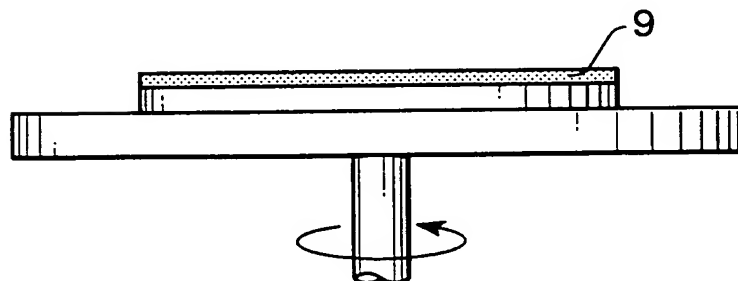
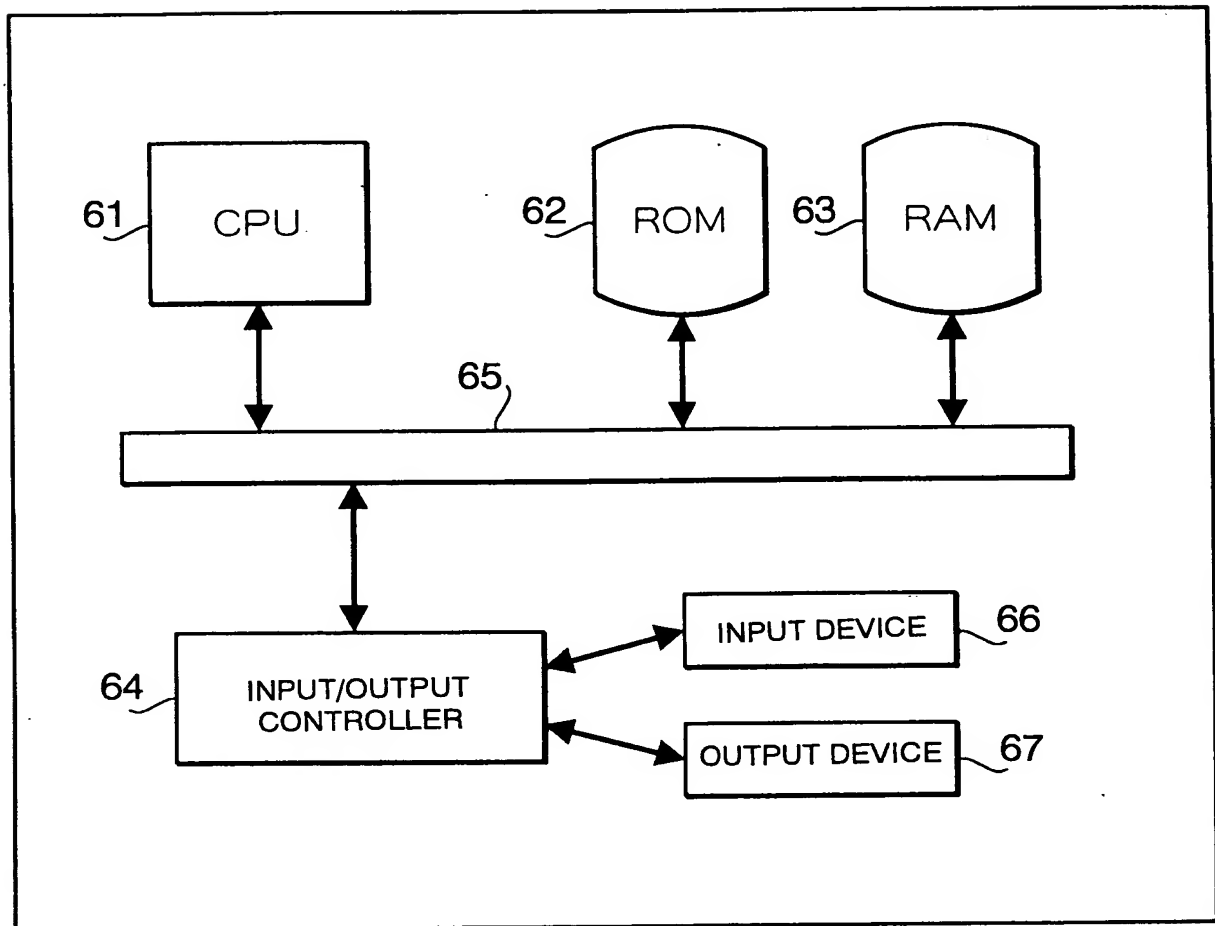


FIG. 6



HOST COMPUTER 60

FIG.7(a)

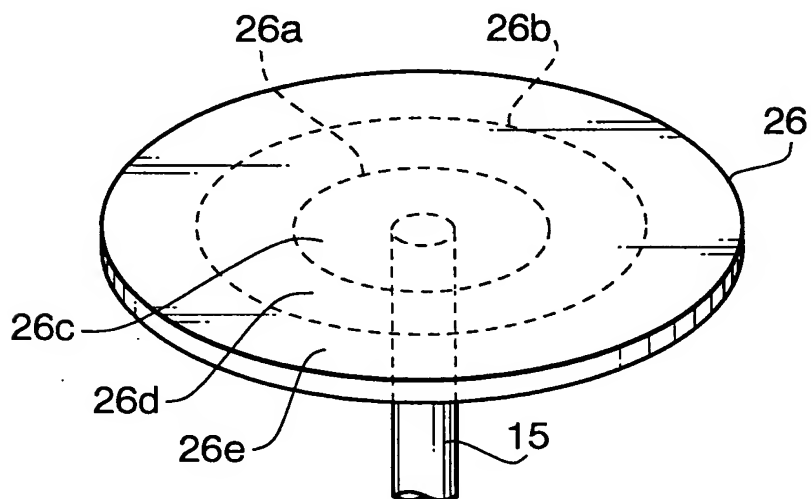


FIG.7(b)

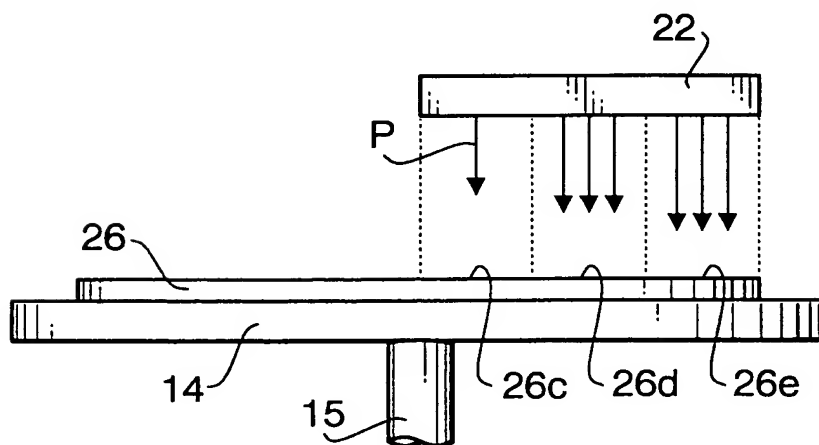


FIG.8(a)

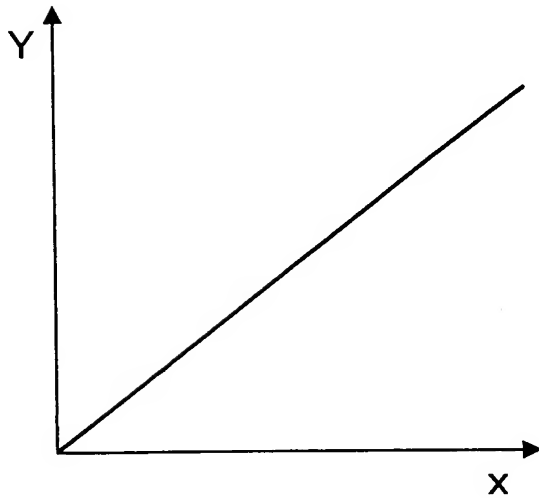


FIG.8(b)

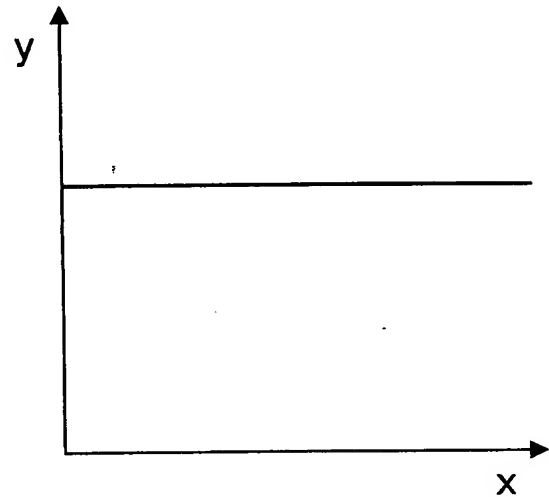


FIG.9(a)

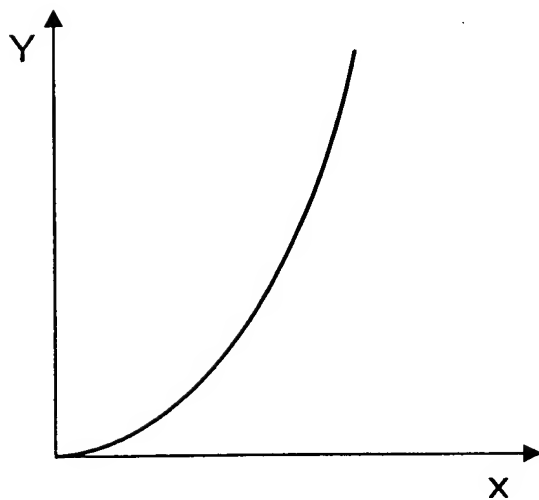


FIG.9(b)

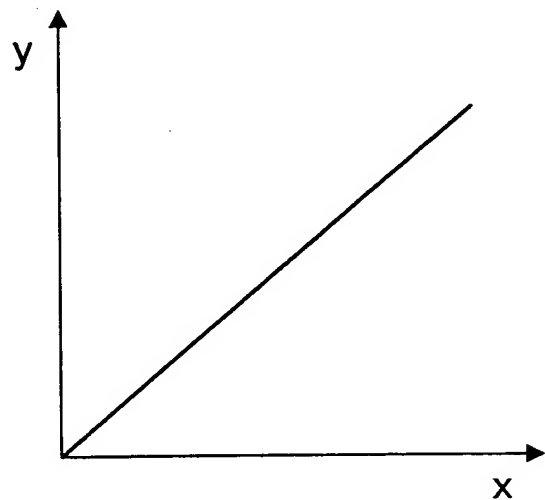




FIG.10(a)

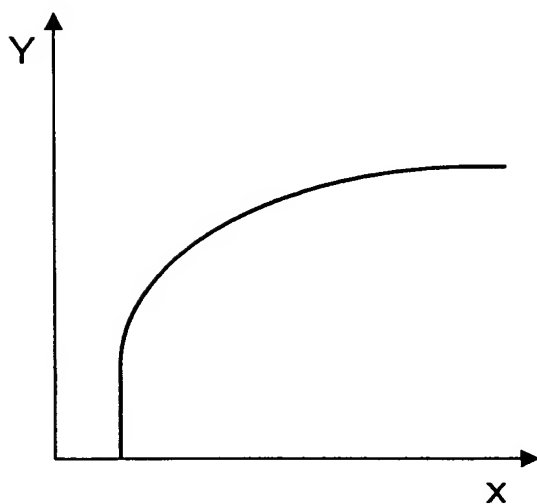


FIG.10(b)

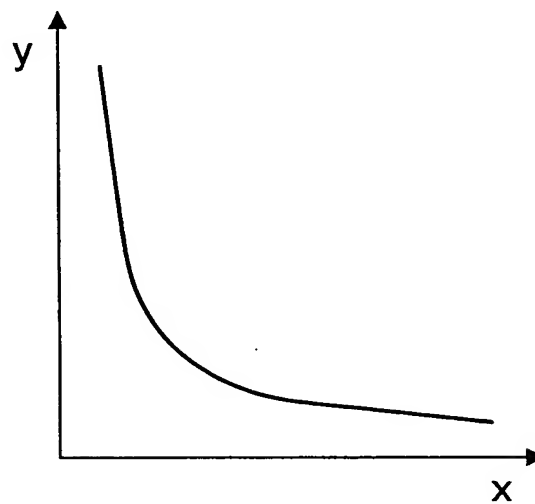


FIG.11(a)

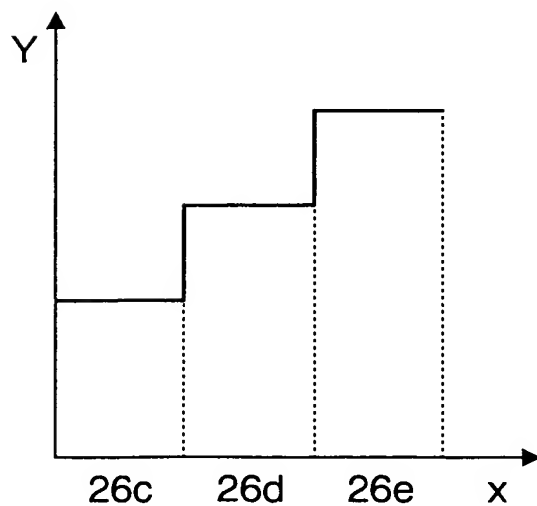


FIG.11(b)

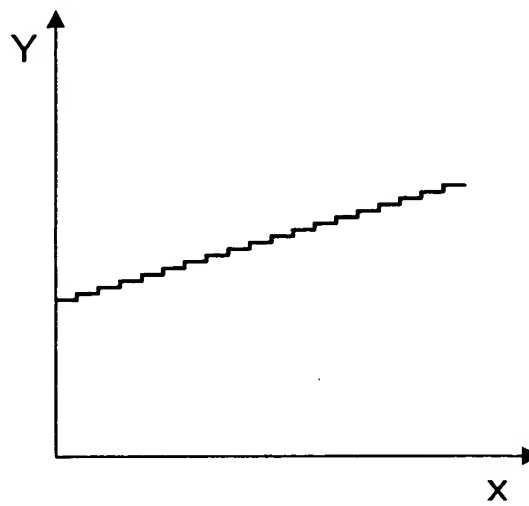


FIG.12

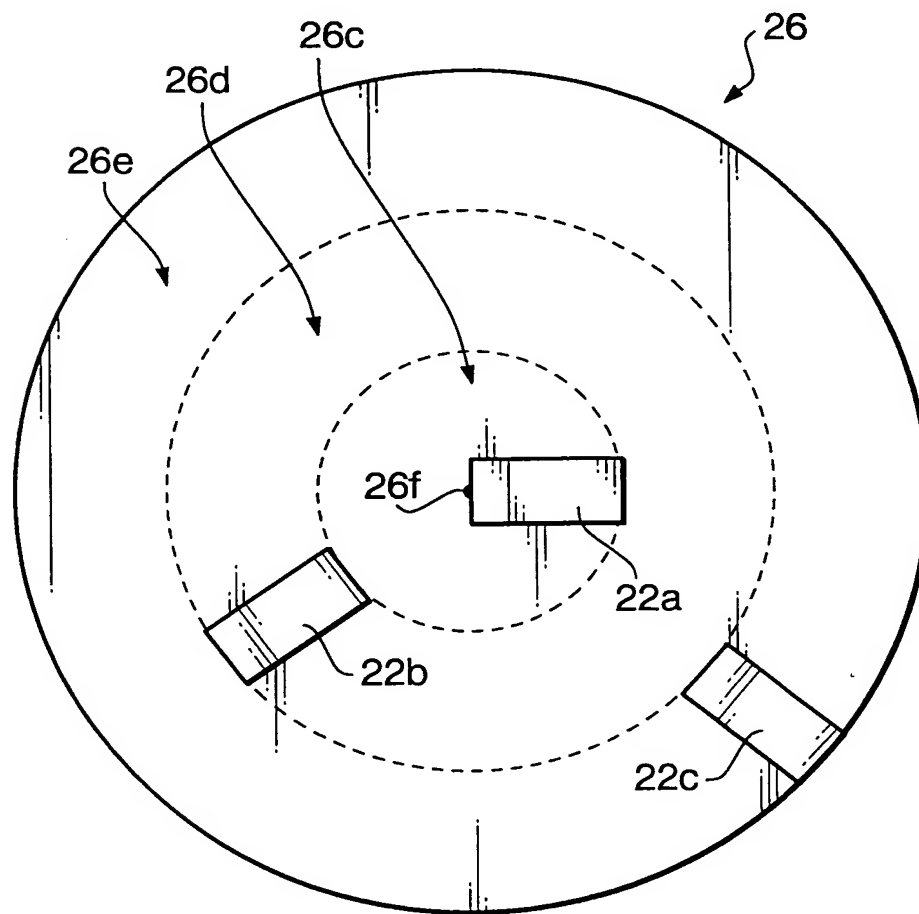


FIG.13

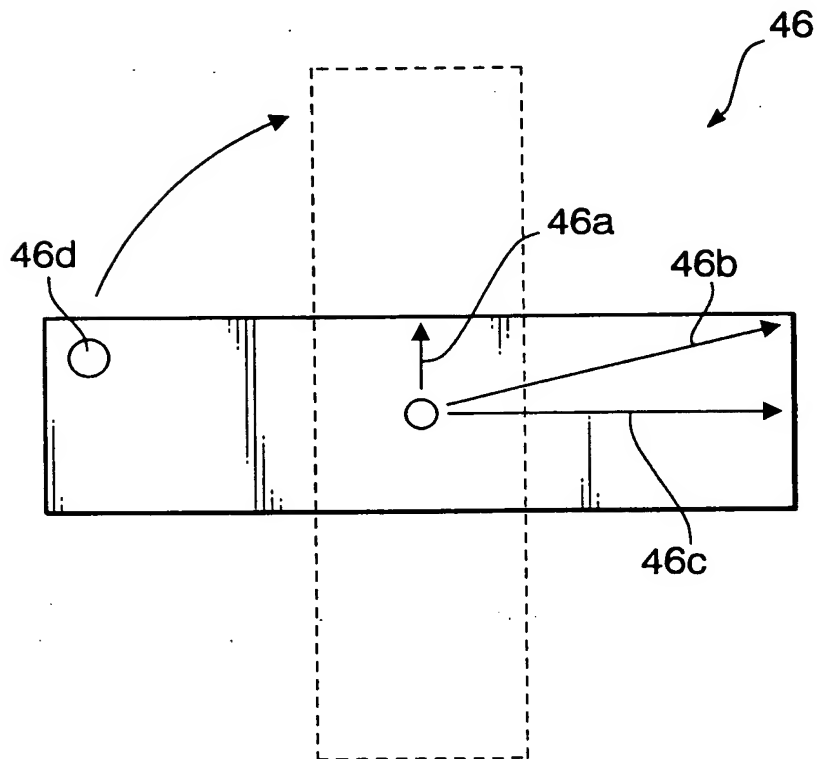


FIG.14(a)

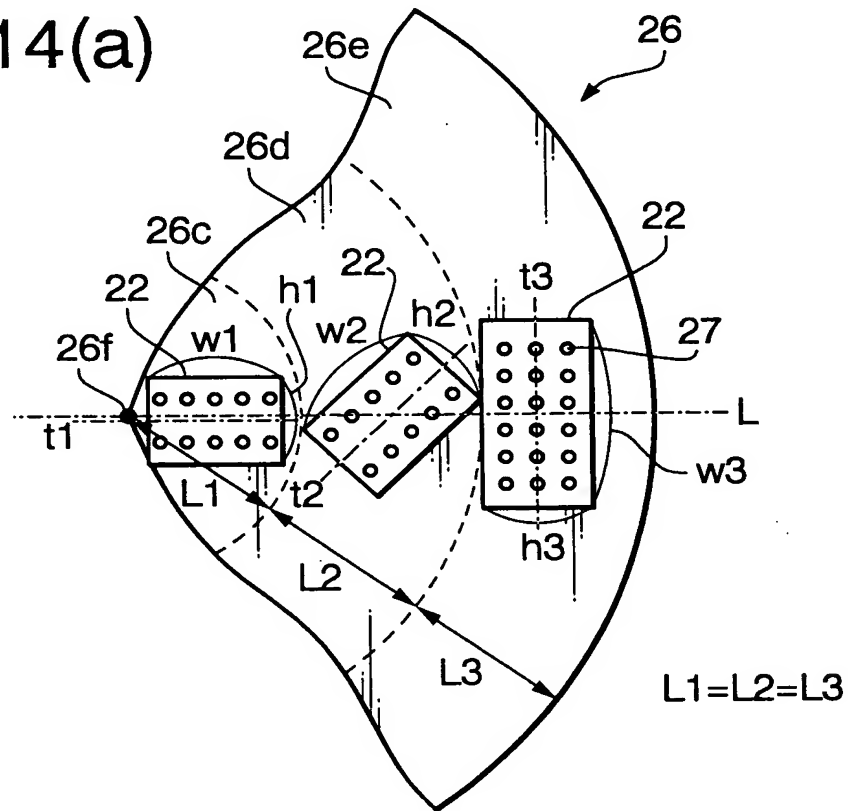


FIG.14(b)

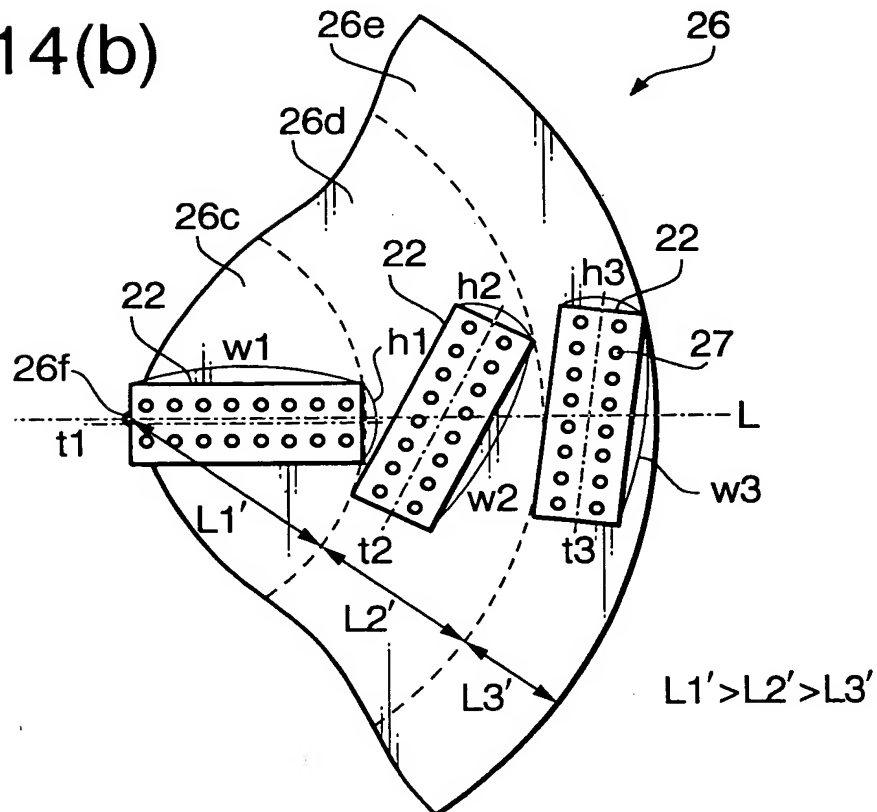


FIG.15

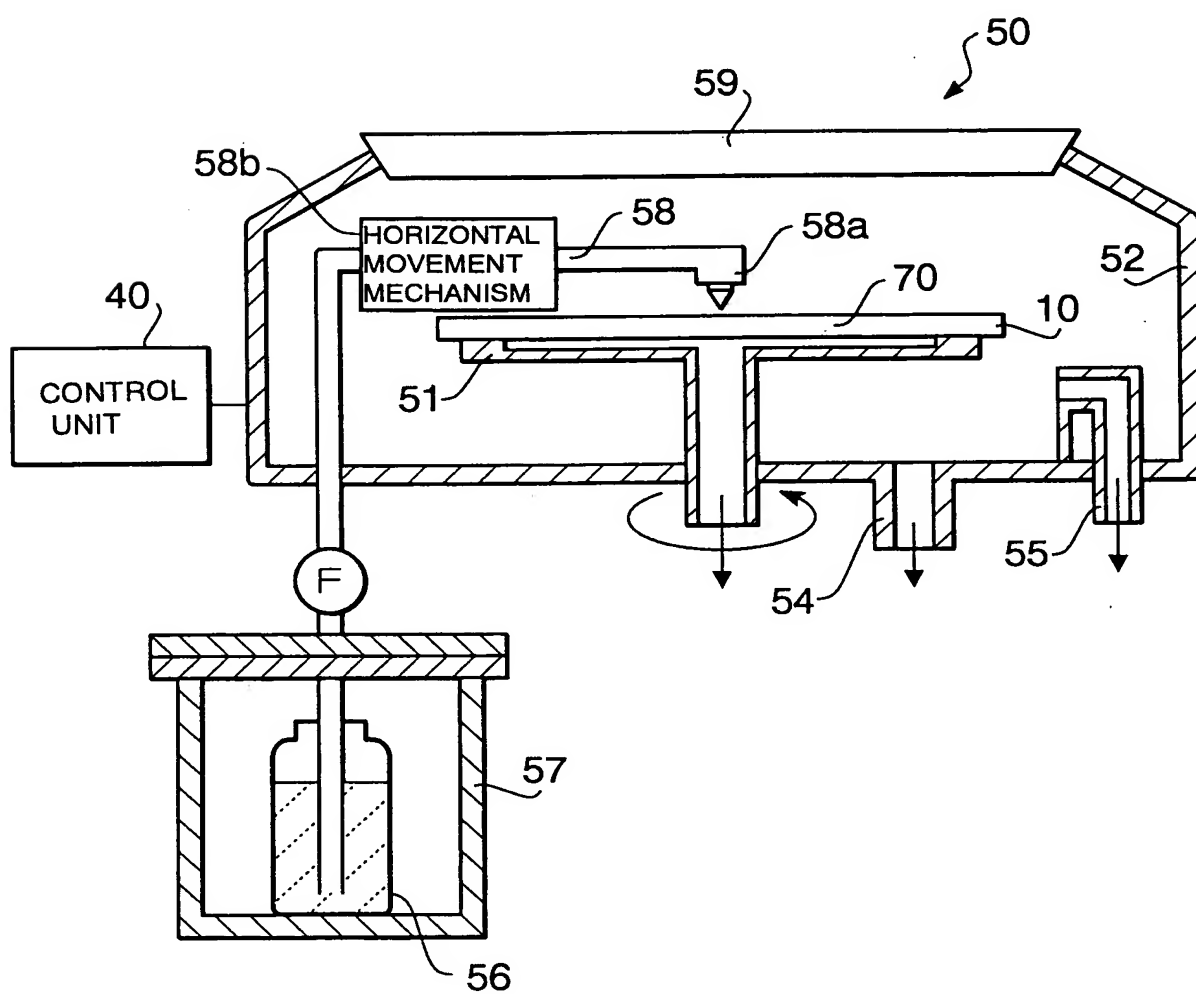
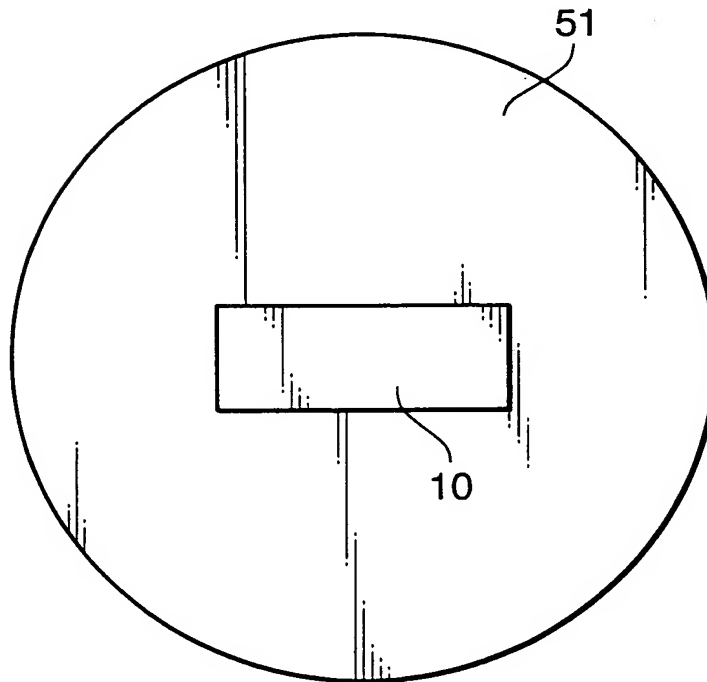
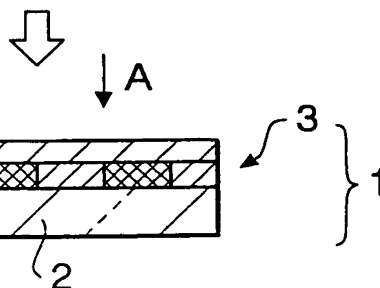
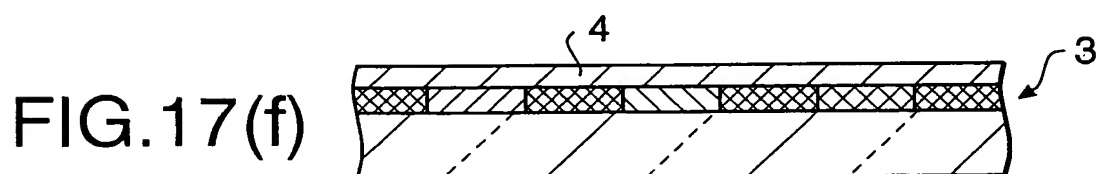
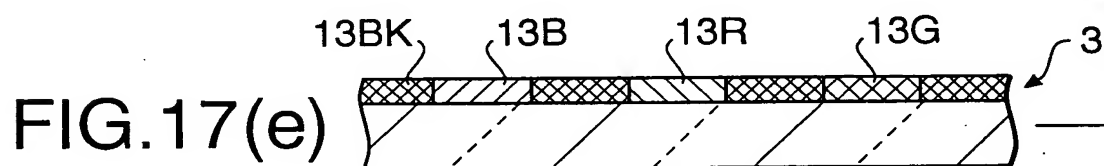
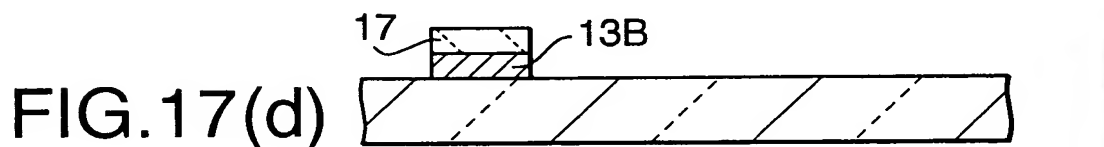
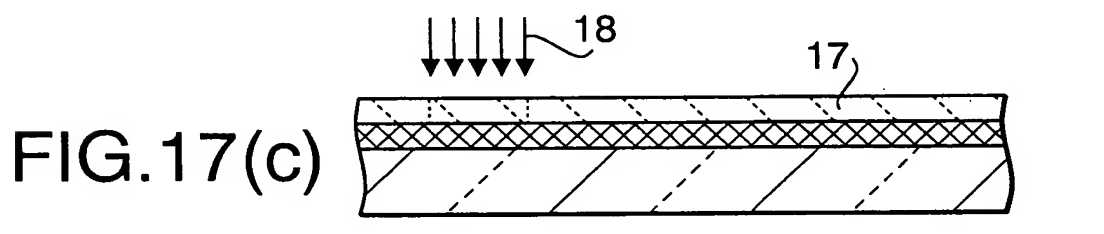
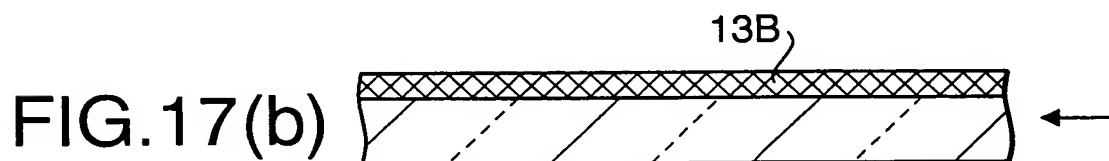
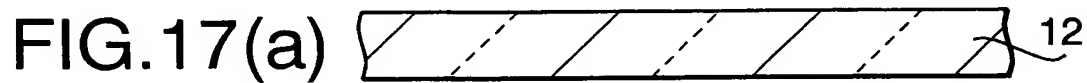


FIG.16





REPEAT 4 TIMES

FIG.18(a)

STRIPE

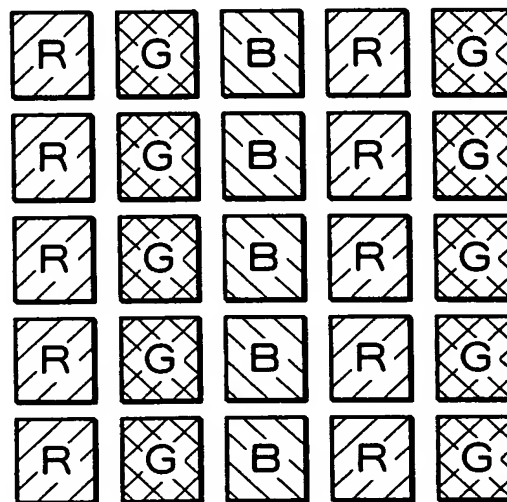


FIG.18(b)

MOSAIC

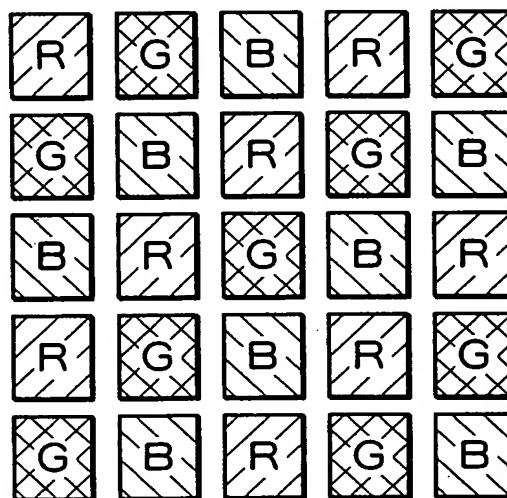


FIG.18(c)

DELTA

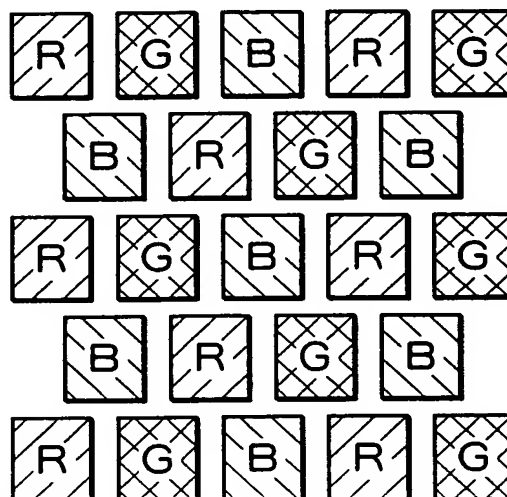




FIG.19

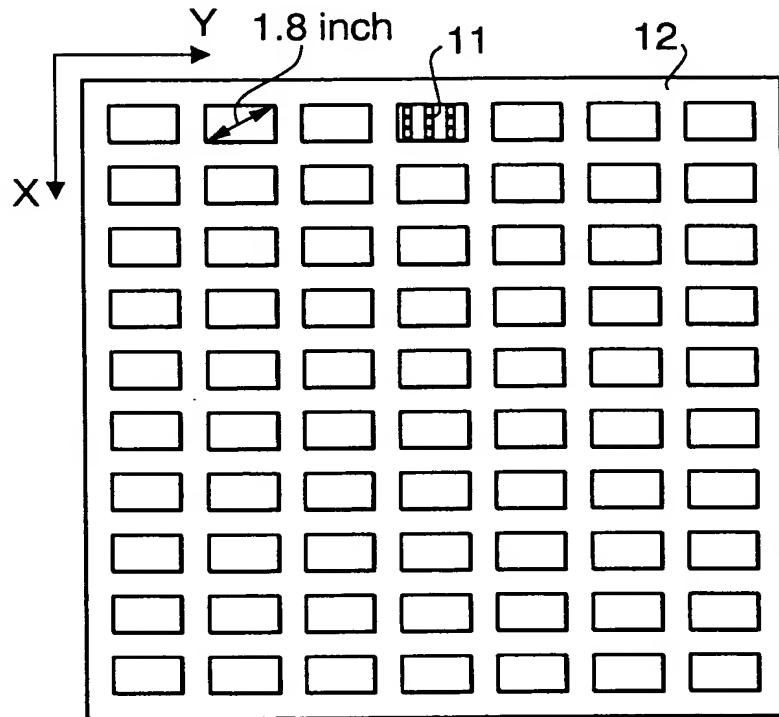


FIG.20

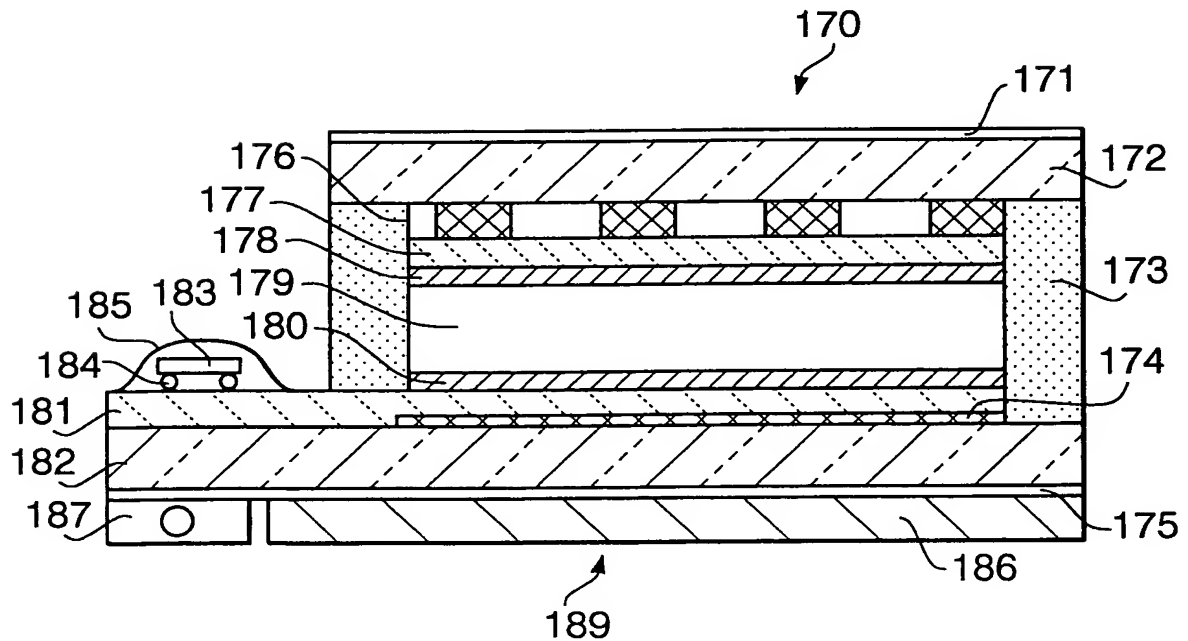


FIG.21

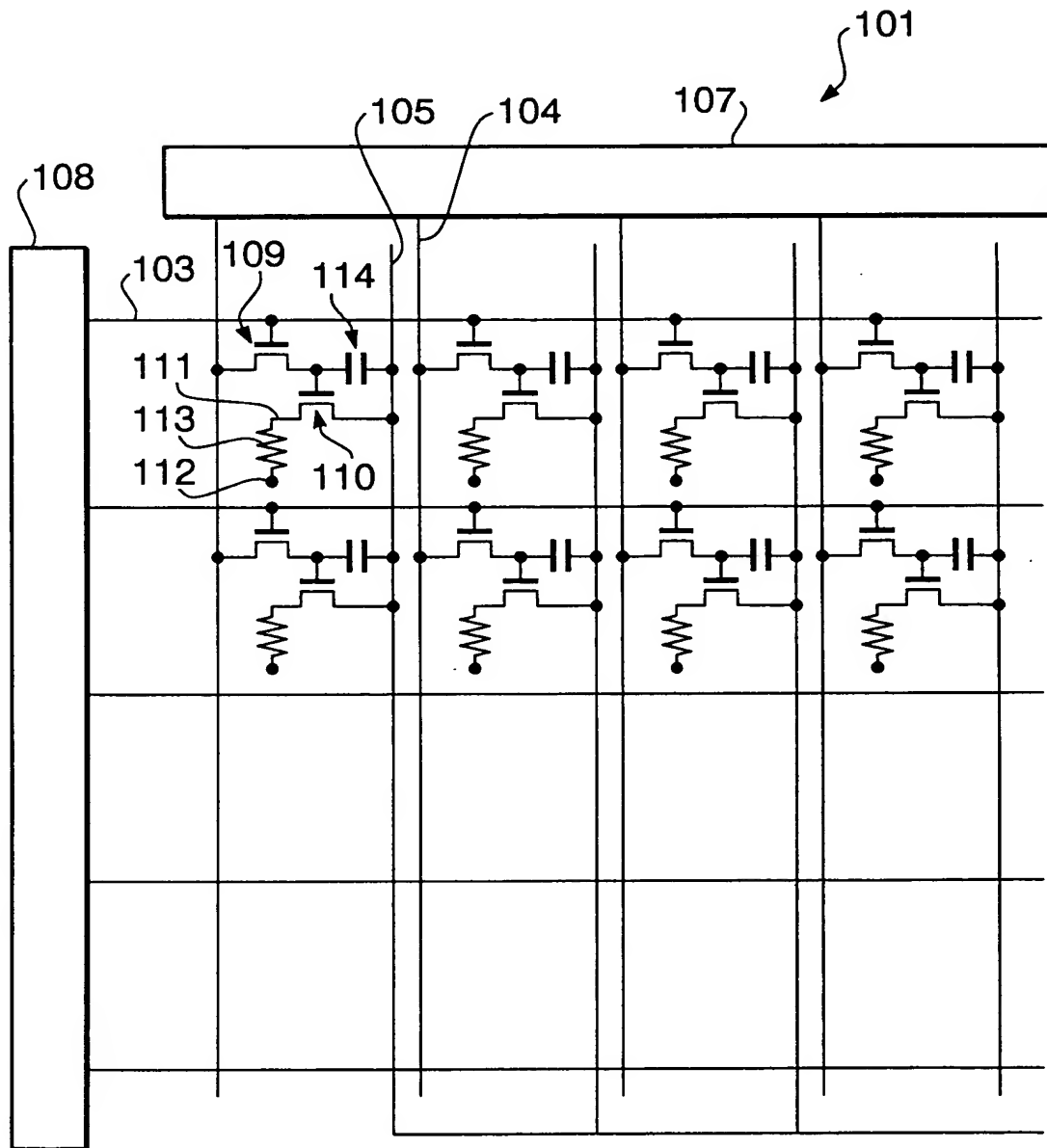


FIG.22(a)

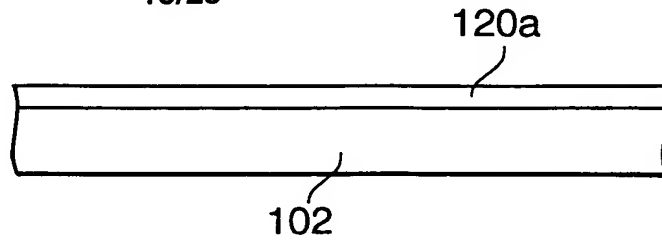


FIG.22(b)

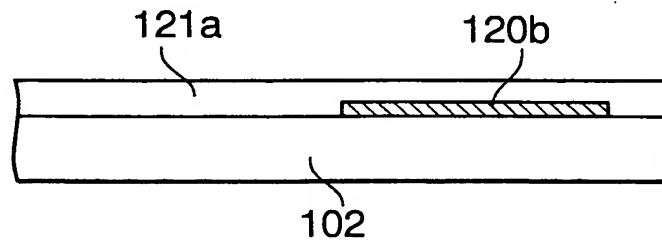


FIG.22(c)

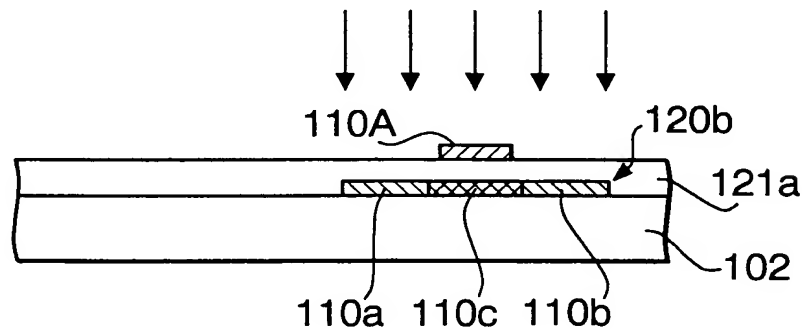


FIG.22(d)

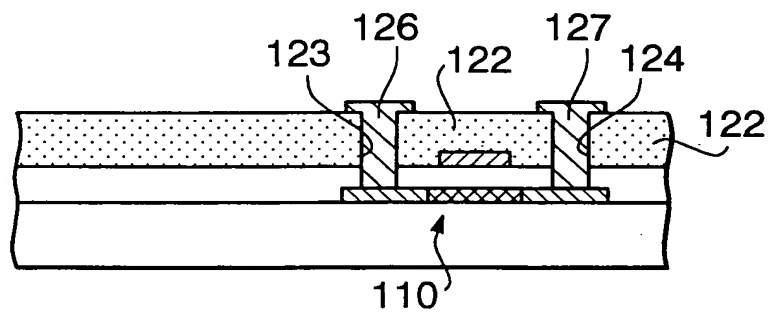


FIG.22(e)

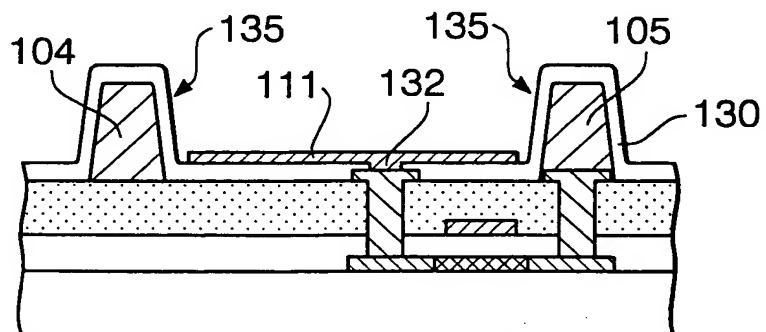


FIG.23(a)

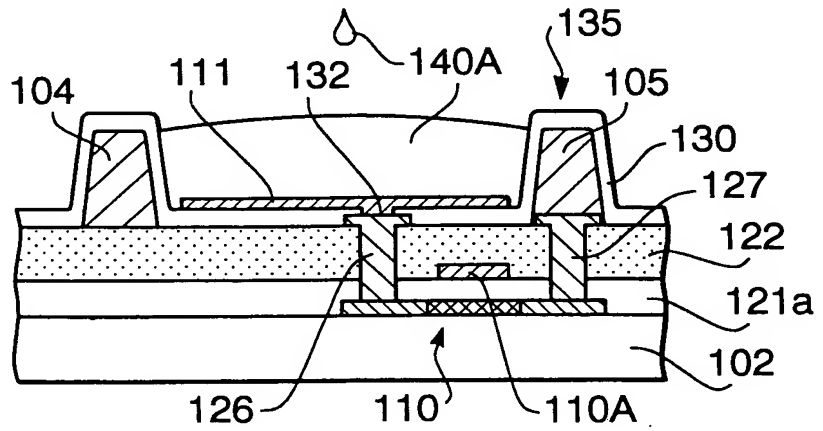


FIG.23(b)

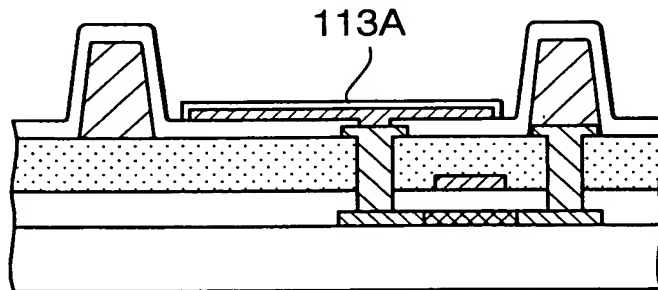
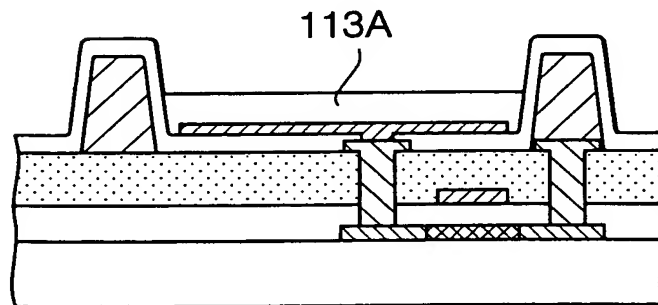


FIG.23(c)



[illegible]

113B

This cross-sectional view shows a gate structure 113B. It features a central gate stack with a core layer and a gate dielectric layer, flanked by side spacers. The gate stack is positioned on a substrate with a patterned layer underneath. The side spacers are shown with a cross-hatched pattern, and the substrate has a dotted pattern. The gate stack is labeled 113B.

A cross-sectional view of a semiconductor device. A gate structure 113 is formed on a substrate. The gate structure 113 includes a gate oxide layer 113A and a gate electrode layer 113B. The gate electrode layer 113B is formed on the gate oxide layer 113A. The gate structure 113 is positioned over a channel region of the substrate. The substrate includes a source region, a drain region, and a channel region. The source region and drain region are formed in the substrate. The channel region is located between the source region and the drain region. The gate structure 113 is positioned over the channel region. The gate oxide layer 113A is formed on the channel region. The gate electrode layer 113B is formed on the gate oxide layer 113A. The gate electrode layer 113B is positioned over the channel region. The gate electrode layer 113B is formed of a conductive material. The gate oxide layer 113A is formed of an insulating material. The gate structure 113 is positioned over the channel region. The gate oxide layer 113A is formed on the channel region. The gate electrode layer 113B is formed on the gate oxide layer 113A. The gate electrode layer 113B is positioned over the channel region. The gate electrode layer 113B is formed of a conductive material. The gate oxide layer 113A is formed of an insulating material.

A cross-sectional view of a semiconductor device. It shows a substrate with a cross-hatched layer labeled 112. This layer is positioned above a base layer and below a top layer. The cross-hatched layer 112 is flanked by two trapezoidal structures with diagonal hatching. Below the cross-hatched layer, there is a layer with a dotted pattern, and further down, a layer with a horizontal line pattern. The entire structure is supported by a base layer with a cross-hatched pattern.

FIG.25

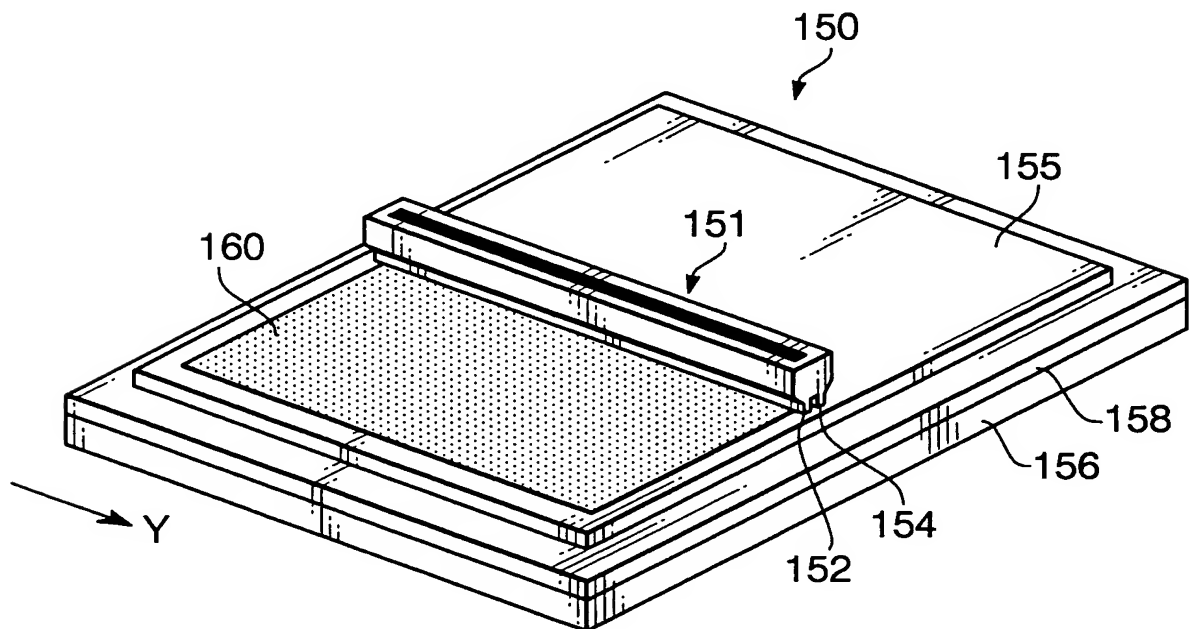


FIG.26  
(PRIOR ART)

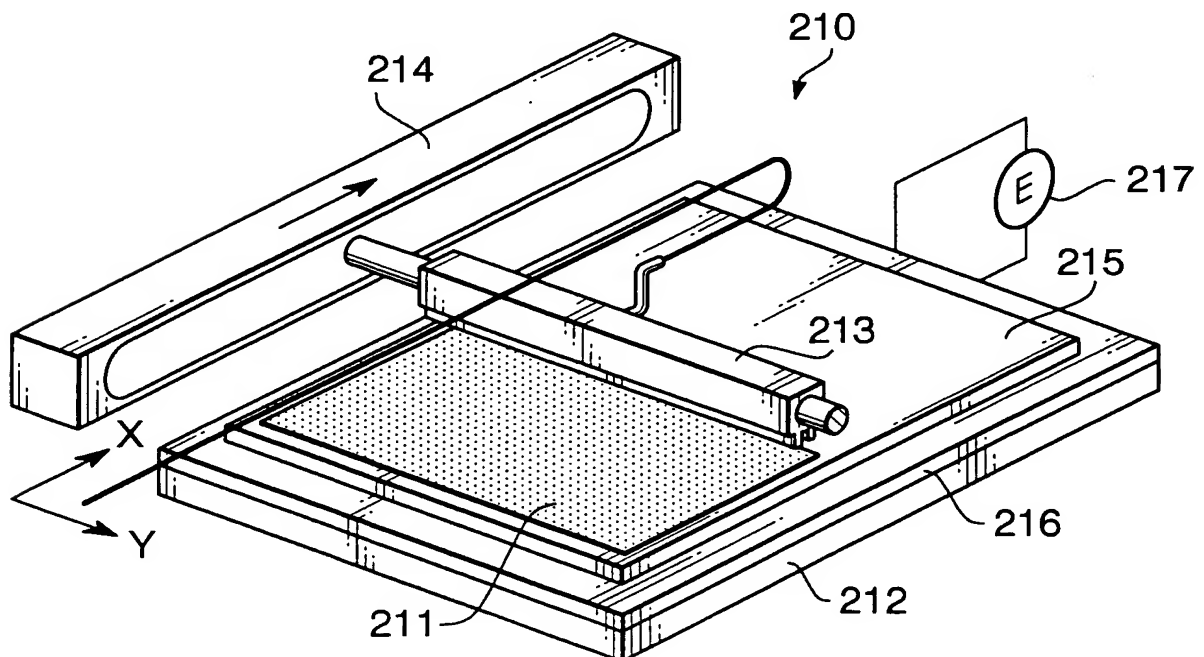


FIG.27  
(PRIOR ART)

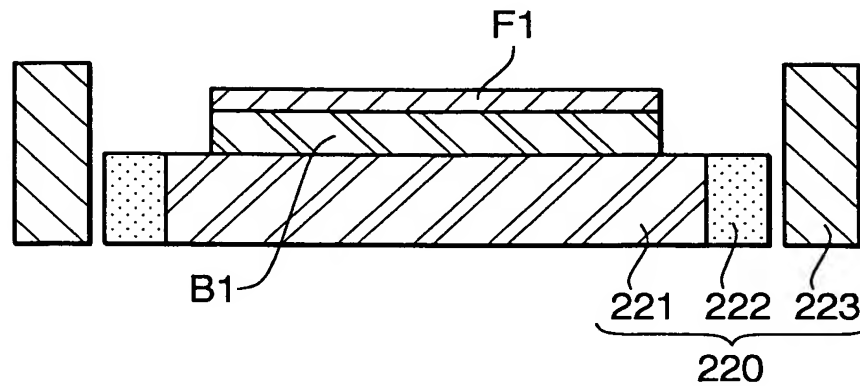


FIG.28  
(PRIOR ART)

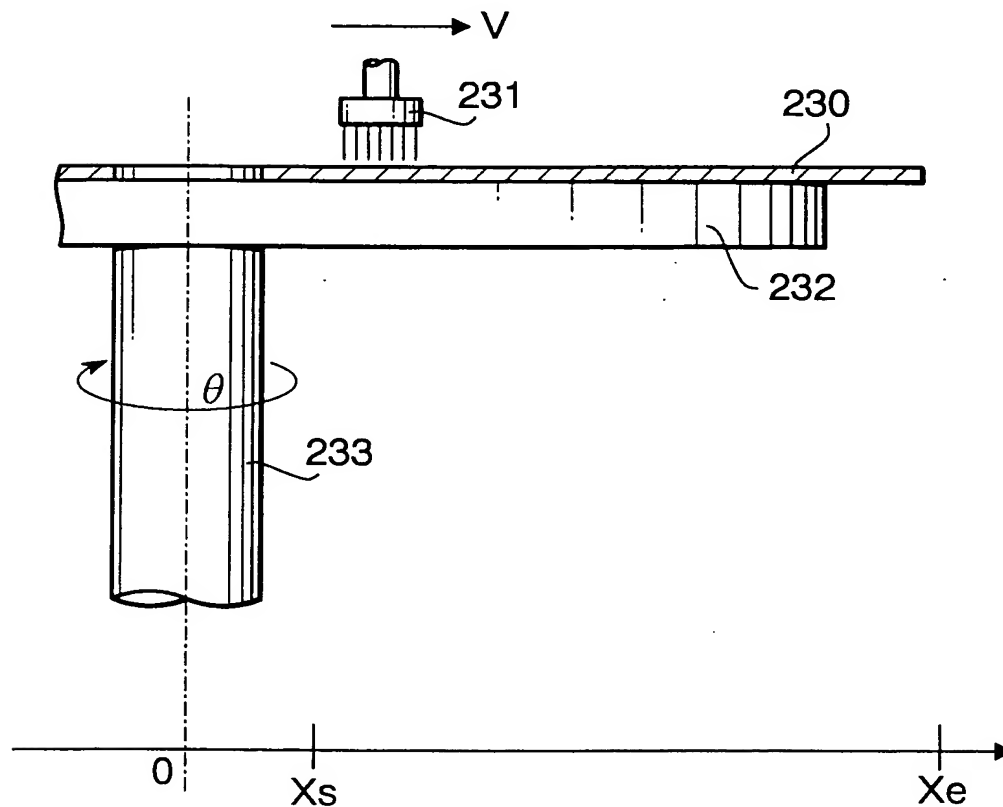


FIG.29  
(PRIOR ART)

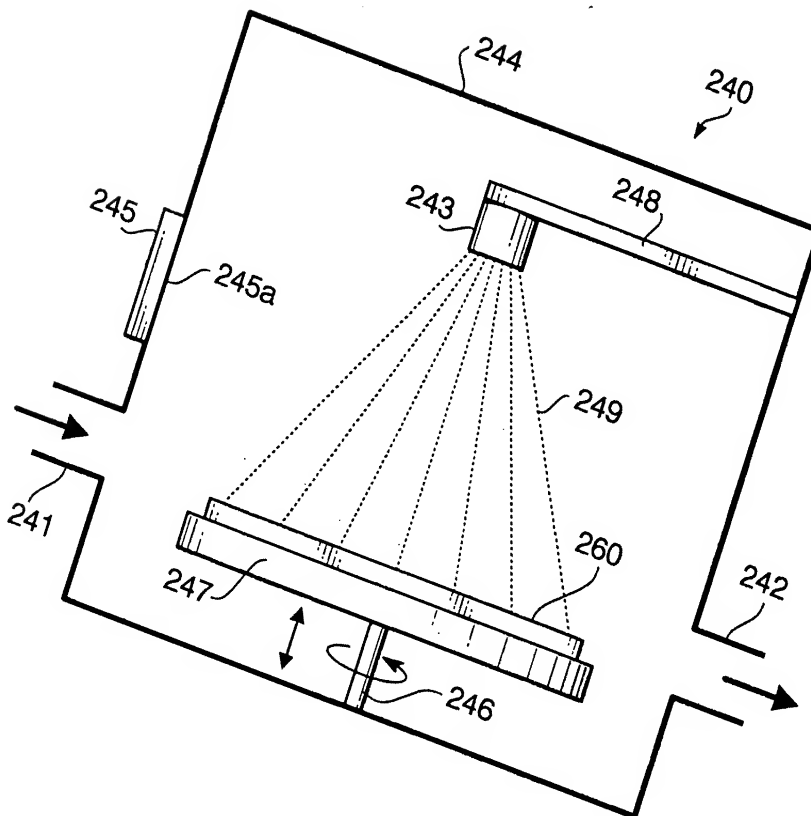




FIG.30  
(PRIOR ART)

